UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,190	11/26/2003	Peter P. Altice JR.	M4065.0852/P852	6553

45374 7590 12/31/2007

DICKSTEIN SHAPIRO LLP
1825 EYE STREET, NW
WASHINGTON, DC 20006

EXAMINER	
BEMBEN, RICHARD M	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
12/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/721,190	ALTICE ET AL.	
	Examiner	Art Unit	
	Richard M. Bemben	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *1,2,5,7-18,30-41 and 44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,6,19-29,42,43 and 45-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1, 2, 8-18, 30-41, drawn to a CMOS image sensor where photodiodes do not share floating diffusion (FD) nodes, i.e. a one-to-one correspondence between photodiodes and FD nodes, classified in class 348, subclass 302 & 308.

   II. Claims 3-7, 19-29 and 42-48, drawn to a CMOS image sensor where plural photodiodes share FD nodes, e.g. 2 photodiodes per FD node or 4 photodiodes per FD node, classified in class 348, subclass 302 & 308.

The inventions are distinct, each from the other because of the following reasons:

2. **Inventions I and II** are directed to a related CMOS image sensor. The related inventions are distinct if the (1) the inventions as claimed are either not capable of use together or can have a materially different design, mode of operation, function, or effect; (2) the inventions do not overlap in scope, i.e., are mutually exclusive; and (3) the inventions as claimed are not obvious variants. See MPEP § 806.05(j). In the instant case, **Inventions I and II** are (1) not capable of use together *and* have a materially different design (Figs. 2-4), mode of operation (Figs. 6-8), function and effect; (2) are mutually exclusive because of the materially different design and operation, such as the

additional capacitor required by **Invention II** at the FD node; and (3) the inventions are not obvious variants.

3. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art due to their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

4. This application contains claims directed to the following patentably distinct species:

Species 1: Figures 3, 7 and 10 directed to 2 photodiodes per FD node (claims 3, 4, 6 and 43)

Species 2: Figures 4, 7, 8, and 11 directed to 4 photodiodes per FD node (claims 5, 7 and 44)

The species are independent or distinct because they at least have a materially different design, mode of operation, and function.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claims 19-29, 42, and 45-48 are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims

readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

5. During a telephone conversation with Jennifer McCue (Reg. No. 55,440) on 18 December 2007 a provisional election was made traverse to prosecute the **Invention II, Species 1**, claims 3, 4, 6, 19-29, 42,43, and 45-48. Affirmation of this election must be made by applicant in replying to this Office action. Claim1, 2, 4, 7-18 and 30-41 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 28 is dependent on independent claim 27. Claim 27 requires each pixel to comprise a reset transistor, a source-follower transistor, and a

row select transistor. Claim 28 requires "pixels" to share a reset transistor, a source-follower transistor, and a row select transistor. It is unclear what constitutes a pixel.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 6, 19, 20 and 23-29, 42, 43, 46, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,731,335 issued to Kim et al., hereinafter "Kim" in view of U.S. 6,522,357 issued to Beiley et al., hereinafter "Beiley".

Claims 3 and 6 are method claims corresponding to apparatus claims 19 and 20. Therefore, claims 3 and 6 are analyzed and rejected as discussed below with respect to claims 19 and 20.

Regarding **claim 19**, Kim discloses a pixel circuit for use in an imaging device, said pixel circuit comprising:

a plurality of photosensors for generating charge during an integration period (c. 4, l. 65 - c. 5, l. 15; Figure 4, "401", "402");

a plurality of transfer gates, each transfer gate connected to and transferring charge from a respective storage node (c. 4, l. 65 - c. 5, l. 15; Figure 4, “M43”, “M44”);

a floating diffusion node connected to said plurality of transfer gates for receiving charge from said transfer gates (c. 4, l. 65 - c. 5, l. 15; Figure 4, "node A" which is the source/drain diffusion of "M1"); and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node (c. 5, ll. 16-24; Figure 4, "M1", "M4").

However, Kim does not disclose a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor and a plurality of storage nodes, each node coupled to a respective shutter transistor and storing charge transferred by a respective one of said plurality of photosensors.

Beiley discloses a well-known CMOS image sensor pixel having an electronic shutter. The pixel comprises a photosensor (Figure 1, "14"), a shutter transistor (Figure 1, "pass transistor M2") connected to and transferring charge from a photosensor to a storage node (Figure 1, "node 2"), the node coupled to a respective shutter transistor and storing charge transferred by the photosensor (Figure 1, charge is stored at "node 2" via "capacitor 34"). Also refer to c. 3, ll. 20-35. Electronic shutters are implemented in digital cameras in order to avoid the additional expense, camera size, and complications that arise out of using a mechanical shutter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include shutter transistors and storage for each photosensor as disclosed by Beiley in the pixel circuit having plural photosensors disclosed by Kim. One would have motivation to do so in order to avoid using a mechanical shutter.

Regarding **claim 20**, refer to the rejection of claim 19 and Kim further discloses that said readout circuit further comprises a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node prior to receiving charge from a respective one said plurality of transfer gates (c. 5, ll. 16-24; Figure 4, "M1").

Regarding **claim 23**, refer to the rejection of claim 19 and Beiley further discloses that said shutter transistor operates as an electronic shutter for said pixels (c. 1, ll. 10-13; c. 3, ll. 20-35).

Regarding **claim 24**, refer to the rejection of claim 19 and Beiley further discloses that said shutter transistor remains on during the integration period (c. 4, ll. 40-61, specifically ll. 49-51).

Regarding **claim 25**, refer to the rejection of claim 19 and Kim further discloses that said pixel is a CMOS pixel (c. 2, ll. 64-67; c. 3, ll. 1-21; Figure 4).

Regarding **claim 26**, the combination of Kim with Beiley discloses a pixel that has five transistors (Kim: Figure 4, "M43, M44, M3"; Beiley: Figure 1, two "M2s").

Regarding **claim 27**, Kim discloses a pixel circuit for use in an imaging device, said pixel circuit comprising:

a photosensor for generating charge during an integration period (c. 4, l. 65 - c. 5, l. 15; Figure 4, "401", "402");

a transfer gate connected to said storage capacitor to transfer charge from said storage capacitor (c. 4, l. 65 - c. 5, l. 15; Figure 4, "M43", "M44");

a floating diffusion node connected to said transfer gate to receive said charge from said transfer gate (c. 4, l. 65 - c. 5, l. 15; Figure 4, "node A" which is the source/drain diffusion of "M1");

a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node (c. 5, ll. 16-24; Figure 4, "M1");

a source-follower transistor connected to said reset transistor for receiving charge from the floating diffusion node (c. 5, ll. 16-24; Figure 4, "M3"); and

a row select transistor connected to said source-follower transistor for outputting a signal produced by said source follower transistor (c. 5, ll. 16-24; Figure 4, "M4").

However, Kim does not disclose a shutter transistor connected to said photosensor to transfer charge from said photosensor and a storage capacitor connected to said shutter transistor to receive said charge transferred by said shutter transistor.

Beiley discloses a well-known CMOS image sensor pixel having an electronic shutter. The pixel comprises a photosensor (Figure 1, "14"), a shutter transistor (Figure 1, "pass transistor M2") connected to and transferring charge from a photosensor to a storage node (Figure 1, "node 2"), the node coupled to a respective shutter transistor and storing charge transferred by the photosensor (Figure 1, charge is stored at "node 2" via "capacitor 34"). Also refer to c. 3, ll. 20-35. Electronic shutters are implemented in digital cameras in order to avoid the additional expense, camera size, and complications that arise out of using a mechanical shutter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

include shutter transistors and storage for each photosensor as disclosed by Beiley in the pixel circuit having plural photosensors disclosed by Kim. One would have motivation to do so in order to avoid using a mechanical shutter.

Regarding **claim 28**, refer to the rejection of claim 27 and Kim further discloses that a plurality of pixel circuits share a floating diffusion node, reset transistor, source follower transistor, and row select transistor (c. 4, l. 65 - c. 5, l. 15; Figure 4, "node A" is shared by "401", "M43" and "402", "M44").

Regarding **claim 29**, refer to the rejection of claim 27 and Kim further discloses that said pixel is a CMOS pixel (c. 2, ll. 64-67; c. 3, ll. 1-21; Figure 4).

Regarding **claim 42**, refer to the rejection of claim 19 over Kim in view of Beiley and Kim further discloses an imaging system comprising a processor (c. 1, ll. 25-60; Figure 1, A/D converter, comparator, CDS, control and interface can all be considered "processors").

Regarding **claim 43**, refer to the rejection of claim 42 and Kim further discloses that a number of said plurality of photosensors is two photosensors (c. 4, l. 65 - c. 5, l. 15; Figure 4, "401", "402").

Regarding **claim 45**, refer to the rejection of claim 42 and Beiley further discloses that said shutter transistor is an electronic shutter (c. 1, ll. 10-13; c. 3, ll. 20-35).

Regarding **claim 46**, refer to the rejection of claim 42 and Beiley further discloses that said shutter transistor remains on during the integration period (c. 4, ll. 40-61, specifically ll. 49-51).

Regarding **claim 48**, refer to the rejection of claim 42 and Kim further discloses that said imaging system is a CMOS imaging system (c. 2, ll. 64-67; c. 3, ll. 1-21; Figure 4).

10. Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Beiley in further view of U.S. Patent No. 6,697,114 issued to Merrill.

Claim 4 is a method claim corresponding to apparatus claim 19. Therefore, claim 4 is analyzed and rejected as discussed below with respect to claim 19.

Regarding **claim 21**, Kim in view of Beiley disclose the limitations of claim 19, specifically storage nodes coupled to shutter transistors for storing charge transferred by photosensors. Beiley further discloses that the storage nodes are capacitors (Figure 1, "34"). While it is well-known that in integrated circuits capacitors are formed using layers of metallization above the substrate in which diffused layers exist, Kim in view of Beiley do not explicitly disclose that the capacitors are formed above the substrate in which the floating diffusion node is formed (diffused within).

Merrill discloses an image sensor pixel having plural photosensors and a shared readout structure where storage capacitors are formed above the substrate in which the floating diffusion node is formed (c. 5, ll. 9-24; "inherent gate capacitances" gate is metallization above the substrate). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form capacitors above the

substrate as disclosed by Merrill in the storage nodes disclosed by Kim in view of Beiley, since that is typically how capacitors are created in integrated circuits.

Allowable Subject Matter

11. Claims 22 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not disclose the use of polypropylene capacitors for use in an electronic shutter circuit of an active pixel sensor.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Nos. 7,238,926, 6,552,323, 6,466,266, 6,423,994, 6,352,869, 6,160,281, 6,107,655 issued to Guidash disclose various pixel structures wherein pixels share output circuits, floating diffusion nodes, reset transistors, etc.

The following disclose pixel structures wherein two or more photosensors share output circuitry:

U.S. Patent No. 7,250,970 issued to Shinohara

U.S. Patent No. 7,244,918 issued to McKee et al.

U.S. Patent No. 6,750,912 issued to Tennant et al.

U.S. Patent No. 7,064,362 issued to Roy

U.S. Patent No. 7,116,367 issued to Shinohara

U.S. Patent No. 7,081,608 issued to Bock

U.S. Patent No. 6,486,913 issued to Afghahi et al.

U.S. Patent No. 6,233,013 issued to Hosier et al.

U.S. Patent No. 6,091,449 issued to Matsunaga et al.

U.S. Patent No. 6,759,641 issued to Loose

U.S. Patent No. 7,053,947 issued to Sohn

U.S. Patent No. 6,867,806 issued to Lee et al.

U.S. Patent No. 5,751,005 issued to Wyles et al.

U.S. Patent No. 5,523,570 issued to Hairston

U.S. Patent No. 6,043,478 issued to Wang

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard M. Bemben whose telephone number is (571) 272-7634. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RMB
12/20/07 RMB 12/20/07

LIN YE
SUPERVISORY PATENT EXAMINER